



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/542,576

07/19/2005

Shinichi Hori

Q89211

6882

23373 7590 01/12/2009
SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER

ROJAS, DANIEL E

ART UNIT

PAPER NUMBER

2816

MAIL DATE

DELIVERY MODE

01/12/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/542,576	Applicant(s) HORI, SHINICHI	
	Examiner DANIEL ROJAS	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 October 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12, 14 and 16-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12, 14 and 16-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 July 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to the objection of claim 19 have been fully considered and are persuasive. The objection of claim 19 has been withdrawn.
2. Applicant's arguments with respect to claims 1-12, 14, and 16-21 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, as required by claim 19, said active device and a second active device comprising said negative resistance device comprising the same type of transistors **having electrical conductivities different from each other** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

Art Unit: 2816

of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-12, 14, and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada (US Patent No. 5,079,443) in view of Donig, hereinafter referred to as Wada and Donig respectively.

7. For claim 1, Wada teaches a voltage-current converting circuit (Figure 2) comprising: an active device (Q21, Q22) having an input terminal (base), an output terminal (collector), and a grounded terminal (emitter, via Q24 and I20), and carrying out

Art Unit: 2816

voltage-current conversion (as explained below); and a resistor circuit (R23, R24, Q23, Q24) electrically connected in series to said active device through said grounded terminal of said active device (as shown), and a voltage-controller (I20) electrically connected to a connection node at which said active device and said resistor circuit are electrically connected to each other (node between I20, Q23 and Q24), wherein said resistor circuit has a variable resistance (inherently based on the structure), and includes a negative resistance device (Q23, Q24) and said voltage-controller controls a voltage of said connection node (via the value of the constant current source) but fails to teach that the voltage-controller compensates for voltage fluctuation caused at said connection node by variance of a resistance of said negative resistance device.

Transistors Q21 and Q22 each input a voltage (V_i and V_B , respectively) and output a current based on said voltage. Therefore, transistors Q21 and Q22 carry out a voltage to current conversion. Donig teaches in his Figure 1 a voltage-controller (LR, Q2) which controls the voltage of a connection node (BK) and compensates for voltage fluctuation caused at said connection node by variance of a resistance at node BK. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use Donig's voltage-controller in place of Wada's I20 in order to regulate the voltage for increased stability. Furthermore, the said combination would have been obvious because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements by known methods at the time of invention with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of invention.

Art Unit: 2816

8. For claim 2, the combination of Wada and Donig as defined above further teaches that said active device is comprised of a pair of active devices (Q21, Q22) each operating differentially with each other (as shown), and each having an input terminal (base terminals of each transistor), an output terminal (collector terminals of each transistor), and a grounded terminal (emitter terminal of each transistor), and carrying out voltage-current conversion (as explained below), said resistor circuit is comprised of a pair of resistor circuits (first: R23, Q23; second: Q22, R24 and both share Donig's Q2 and LR, as explained below) each electrically connected in series to each of said active devices through said grounded terminal of each of said active devices (as shown), and each controlling a conversion gain of each of said active devices (inherent based upon the structure), each of said resistor circuits having a variable resistance (as explained below), and including a negative resistance device (Q23 and Q24, respectively).

Transistors Q21 and Q22 input a voltage (V_A and V_B , respectively) and output a current based on voltage. Therefore, Q21 and Q22 carry out a voltage to current conversion.

T2 is defined by Donig as a controllable resistor, hence a variable resistor (column 4, lines 16-20), which in the combinational circuit of Wada and Donig, compensates for both of the pairs of resistor circuits. Since the gates of Q23 and Q24 are directly affected by the value of Donig's LR, the negative resistance devices' resistance value is dependent on the value of LR. Therefore, since each of said resistor circuit comprises a negative resistor, each of said resistor circuits has a variable resistance.

9. For claim 3, as explained above, the gates of Q23 and Q24 are directly affected by the value of Donig's LR and the negative resistance devices' resistance value is

Art Unit: 2816

dependent on the value of LR. Therefore, said negative resistance device has a negative resistance.

10. For claim 4, the combination of Wada and Donig as defined above further teaches that said resistor circuit is comprised of: one or a plurality of resistance device(s) electrically connected in series to said active device (R22); and said negative resistance device electrically connected in parallel with at said resistance device (as explained below). Resistor R22 and transistor Q23 are both connected between V_{CC} and ground and are therefore in parallel.

11. For claim 5, the combination of Wada and Donig as defined above further teaches that wherein said resistor circuit is comprised of a first circuit comprised of a resistance device (R24) and a negative resistance device (Q24) electrically connected in series to each other, said first circuit being electrically connected in series to said active device (as shown).

12. For claim 6, the combination of Wada and Donig as defined above further teaches that said resistor circuit is comprised of a first resistance device (R22) electrically connected in series to said active device, and a second circuit electrically connected in parallel with said first resistance device (Q23), said second circuit being comprised of a-said negative resistance device (as explained above), and a second resistance device (R23) electrically connected in series to said negative resistance device. Resistor R22 and transistor Q23 are both connected between V_{CC} and ground and are therefore in parallel.

Art Unit: 2816

13. For claim 7, the combination of Wada and Donig as defined above further teaches that said negative resistance device of said pair of resistance circuits is comprised of a pair of active devices (Q23 and Q24) electrically connected in cross to each other and operating differentially with each other (inherent based upon the structure), and each receiving, as an input signal, a node signal either at a connection node at which said active device and said resistor circuit are electrically connected to each other or at any connection node in said resistor circuit (as shown).

14. For claim 8, the modified version of Wada as defined above further teaches that said negative resistance device is comprised of a bipolar transistor (BJTs Q23 and Q24)

15. For claim 9, the modified version of Wada as defined above further teaches that a resistance of said negative resistance device is controlled by controlling either a source voltage or an emitter voltage of said field effect transistor or bipolar transistor (inherent based upon the structure).

16. For claim 10, the modified version of Wada as defined above further teaches a voltage-providing circuit (Donig's Q2, as defined above) electrically connected between a reference voltage point (ground) and either a source or an emitter of said field effect transistor or bipolar transistor (as shown), and wherein a resistance of said negative resistance device is controlled by controlling a voltage provided by said voltage-providing circuit (as shown).

17. For claim 11, Wada teaches a circuit (Figure 2) comprising an active device (Q21, Q22) having an input terminal (base), an output terminal (collector), and a grounded terminal (emitter), and carrying out voltage-current conversion; and a resistor

Art Unit: 2816

circuit (R23, R24, Q23, Q24) electrically connected in series to said active device through said grounded terminal of said active device (as shown), and controlling a conversion gain of said active device (inherent based upon the structure), said resistor circuit including a negative resistance device (Q23, Q24) wherein said negative resistance device is comprised of a field effect transistor or a bipolar transistor (as shown), wherein a resistance of said negative resistance device is controlled by controlling either a source voltage or an emitter voltage of said field effect transistor or bipolar transistor (inherent based upon the structure), wherein said voltage-current converting circuit further comprises a voltage-providing circuit (I20) electrically connected between a reference voltage point (GND) and either a source or an emitter of said field effect transistor or bipolar transistor (as shown) but fails to teach that said resistor circuit has a variable resistance and that a resistance of said negative resistance device is controlled by controlling a voltage provided by said voltage-providing wherein said voltage providing circuit comprises an operational amplifier having a first input terminal, a second input terminal, and an output terminal; and an active device, wherein a voltage-control signal is input to said first input signal of said operational amplifier, an input terminal of said active device is electrically connected to said output terminal of said operational amplifier, and an output terminal of said active device is electrically connected to said second input terminal of said operational amplifier. However, Donig teaches a voltage regulating/providing circuit (Q2) based on a regulation voltage (UR). It would have been obvious to one of ordinary skill in the art at the time of invention to use Donig's voltage regulating/providing circuit (LR) in place

Art Unit: 2816

of Wada's voltage providing circuit (I20) in order to regulate the voltage for increased stability. Furthermore, the said combination would have been obvious because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements by known methods at the time of invention with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of invention. The combination circuit of Wada and Donig teaches that a resistance of said negative resistance device is controlled by controlling a voltage provided by said voltage-providing circuit (inherent based upon the structure) wherein said voltage providing circuit comprises an operational amplifier (OP1) having a first input terminal, a second input terminal, and an output terminal (as shown); and an active device (T2), wherein a voltage-control signal is input to said first input signal of said operational amplifier (as shown), an input terminal of said active device is electrically connected to said output terminal of said operational amplifier (as shown), and an output terminal of said active device is electrically connected to said second input terminal of said operational amplifier (as shown).

18. For claim 12, the combination of Wada and Donig as defined above further teaches that said negative resistance device is comprised of a pair of bipolar transistors (Q23 and Q24) operating differentially with each other (as shown), wherein sources or emitters of said field effect transistors or bipolar transistors are electrically connected to each other (as shown).

19. For claim 14, the combination of Wada and Donig as defined above further teaches that said voltage controller is comprised of an active device (T2) electrically

Art Unit: 2816

connected between a reference voltage (GND) and said connection node, and having an input terminal to which a bias signal is input (gate terminal).

20. For claim 16, the combination of Wada and Donig as defined above further teaches that said resistor circuit includes a variable resistor (T2) having a positive resistance (as explained below) When the signal applied to the gate of T2 increases, the resistance value of T2 also increases proportionally.

21. For claims 17 and 18, the combination of Wada and Donig as defined above further teaches that said variable resistor is comprised of an active device (NMOS transistor).

22. For claim 19, combination of Wada and Donig as defined above teaches the circuit of claim 1 but fails to teach the limitations of claim 19. Examiner takes official notice that p-type transistors can be substituted for n-type transistors and vice versa. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention that Wada's active device and negative resistance device can be implemented as transistors of electrical conductivities different from each other since the substitution of one known element for another would have yielded predictable results to one of ordinary skill in the art at the time of invention.

23. For claim 20, Wada teaches in his Figure 2 a circuit including a combination circuit comprised of a voltage-current converting circuit, , wherein a pass band is controlled by varying a gain of said voltage-current converting circuit (inherent based upon the structure), said voltage-current converting circuit comprising: an active device (Q22) having an input terminal (base), an output terminal (collector), and a grounded

Art Unit: 2816

terminal (emitter), and carrying out voltage-current conversion (inherent based upon the structure) and a resistor circuit (R23, R24, Q23, Q24) electrically connected in series to said active device through said grounded terminal of said active device, controlling a conversion gain of said active device (inherent based upon the structure), said resistor circuit comprising a negative resistance device (Q23 and Q24) but fails to teach that said resistor circuit having a variable resistance and a capacity device. Transistors Q21 and Q22 each input a voltage (V_i and V_B , respectively) and output a current based on said voltage. Therefore, transistors Q21 and Q22 carry out a voltage to current conversion. Donig teaches in his Figure 1 a voltage-controller (LR, Q2) which controls the voltage of a connection node (BK) and compensates for voltage fluctuation caused at said connection node by variance of a resistance at node BK. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use Donig's voltage-controller in place of Wada's I20 in order to regulate the voltage for increased stability. Furthermore, the said combination would have been obvious because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements by known methods at the time of invention with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of invention. The combination of Wada and Donig as defined above teaches a resistor circuit having a variable resistance (T2) and a capacity device (within the loop filter LF).

24. For claim 21, Wada teaches a circuit which outputs a current in accordance with the voltage thereto (via Q21, Q22), comprising: an active device (Q21, Q22) having an

Art Unit: 2816

input terminal (base), an output terminal (collector), and a grounded terminal (emitter), and carrying out voltage-current conversion (inherently); a resistor circuit (R23, R24, Q23, Q24) electrically connected in series to said active device through said grounded terminal of said active device (as shown), and controlling a conversion gain of said active device (inherently based upon the structure), wherein said resistor circuit includes a negative resistance device (Q23, Q24), said negative resistance device comprises a field effect transistor or a bipolar transistor, a resistance of said negative resistance device is controlled by controlling either a source voltage or an emitter voltage of said field effect transistor or said bipolar transistor (inherent based upon the structure); said voltage-current converting circuit further comprising a voltage-providing circuit (I20) electrically connected between a reference voltage point (GND) and either a source or an emitter of said field effect transistor or said bipolar transistor (as shown); but fails to teach that the resistor circuit has a variable resistance and that a resistance of said negative resistance device is controlled by controlling a voltage provided by said voltage-providing circuit, wherein said voltage providing circuit comprises: an operational amplifier having a first input terminal, a second input terminal, and an output terminal; and an active device, wherein a voltage-control signal is input to said first input signal of said operational amplifier, an input terminal of said active device is electrically connected to said output terminal of said operational amplifier, and an output terminal of said active device is electrically connected to said second input terminal of said operational amplifier. Transistors Q21 and Q22 each input a voltage (V_i and V_B , respectively) and output a current based on said voltage. Therefore, transistors Q21

Art Unit: 2816

and Q22 carry out a voltage to current conversion. Donig teaches in his Figure 1 a voltage-controller (LR, Q2) which controls the voltage of a connection node (BK) and compensates for voltage fluctuation caused at said connection node by variance of a resistance at node BK. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use Donig's voltage-controller in place of Wada's I20 in order to regulate the voltage for increased stability. Furthermore, the said combination would have been obvious because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements by known methods at the time of invention with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of invention. The combination of Wada and Donig as defined above teaches that the resistor circuit has a variable resistance (T2) and that a resistance of said negative resistance device is controlled by controlling a voltage provided by said voltage-providing circuit (LR and Q2), wherein said voltage providing circuit comprises: an operational amplifier (OP1) having a first input terminal, a second input terminal, and an output terminal (as shown); and an active device (T2), wherein a voltage-control signal is input to said first input signal of said operational amplifier (UR), an input terminal of said active device is electrically connected to said output terminal of said operational amplifier (as shown), and an output terminal of said active device is electrically connected to said second input terminal of said operational amplifier (as shown).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL ROJAS whose telephone number is (571)270-5070. The examiner can normally be reached on Monday-Friday 7:30-8 EST, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan Lam/
Primary Examiner, Art Unit 2816

/D. R./
Examiner, Art Unit 2816
1/7/2009